ABSTRACT

In this invention, a control circuit (111) controls both the power supply voltage (VDDQ) and the transistor size of the external output buffer to thereby select the lowest supply voltage that achieves the impedance matching with the transmission line (100), to thereby save bus termination by a resistor, thus consequently achieving both the lowering of the power consumption and the speeding-up in the data transmission. The power consumption during the data transmission is proportional to the square of the supply voltage. If the operational supply voltage of the external output buffer is lowered, the power consumption will be reduced accordingly. If the operational supply voltage of the external output buffer is lowered, the impedance thereof will be increased apparently; and at the same time, if the transistor size of the external output buffer is increased, the increased impedance will be decreased. By bringing the output impedance (ON-resistance) of the external output buffer into conformity with the impedance of the transmission line, it becomes possible to output the signal without distortions on the waveform.